## APPEAL BRIEF UNDER 37 C.F.R. § 41.37

TABLE OF CONTENTS

**PATENT**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application of: Paul A. Farrar — Examiner: Dilinh P. Nguyen

Serial No.: 09/259,849 — Group Art Unit: 2814

Filed: March 1, 1999 — Docket: 303.557US1

For: CONDUCTIVE STRUCTURES IN INTEGRATED CIRCUITS

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# APPEAL BRIEF UNDER 37 CFR § 41.37

Mail Stop Appeal Brief- Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The Appeal Brief is presented in support of the Notice of Appeal to the Board of Patent Appeals and Interferences, filed on February 8, 2006, from the Final Rejection of claims 1-7, 12-44, 50-77 and 186-189 of the above-identified application, as set forth in the Final Office Action mailed on September 8, 2005.

The Commissioner of Patents and Trademarks is hereby authorized to charge Deposit Account No. 19-0743 in the amount of 500.00 which represents the requisite fee set forth in 37 C.F.R. § 41.2(b)(2). The Appellants respectfully request consideration and reversal of the Examiner's rejections of pending claims.

## 1. REAL PARTY IN INTEREST

The real party in interest of the above-captioned patent application is the assignee, MICRON TECHNOLOGY, INC..

## 2. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellant that will have a bearing on the Board's decision in the present appeal.

## 3. STATUS OF THE CLAIMS

The present application was filed on March 1, 1999 with claims 1-185. Claims 186-189 were added in an Amendment filed March 25, 2003. Claims 1-7, 12-44 50-77 and 186-189 stand twice rejected and are the subject of the present Appeal; claims 45-49 were allowed; claims 8-11 and 78-185 were previously canceled.

## 4. STATUS OF AMENDMENTS

No amendments have been made subsequent to the Final Office Action dated September 9, 2005.

## 5. SUMMARY OF CLAIMED SUBJECT MATTER

Some aspects of the present inventive subject matter include, but are not limited to, methods of forming a conductive structure.

Some embodiments include a method of forming a conductor comprising depositing an insulator (125) over a planarized surface; etching a trench (130) having a depth on the insulator; depositing a barrier layer (135) on the insulator; depositing a seed layer (140) directly on the barrier layer; removing the barrier layer and seed layer from selected areas (160) of the insulator, leaving a seed area (155); and depositing a conductor (145) on the seed area by a selective deposition process after removing the barrier layer and seed layer from selected areas of the insulator; wherein the selected areas are directly on a top surface of the insulator. Page 6, line 18 through page 9, line 2, Fig. 1.

Some embodiments include a method of forming a conductor comprising depositing an oxide layer (125) over a planarized surface; etching a trench (130) on the oxide layer; depositing a barrier layer (135) on the oxide layer; depositing a seed layer (140) on the barrier layer without a layer between the seed layer and the barrier layer; removing the barrier layer and seed layer from unused areas (160) of the oxide layer, leaving a seed area (155); and depositing a conductor (145) on the seed area after removing the barrier layer and seed layer from unused areas of the oxide layer; wherein the unused areas are directly on a top surface of the oxide layer. Page 6, line 18 through page 9, line 2, Fig. 1.

Some embodiments include a method of forming a conductor comprising depositing an oxide layer (125) over a planarized surface; etching a trench (130) on the oxide layer; depositing a barrier layer (135) of tantalum on the oxide layer; depositing a seed layer (140) selected from the group consisting of gold, silver, and copper on the oxide layer; removing the barrier layer of tantalum and seed layer from unused areas (160) of the oxide layer, leaving a seed area (155); and depositing a conductor (145) on the seed area after removing the barrier layer of tantalum and seed layer from unused

areas of the oxide layer; wherein the unused areas are directly on a top surface of the oxide layer. Page 6, line 18 through page 9, line 2, Fig. 1.

Some embodiments include a method of forming a conductor comprising depositing an oxide layer (125) over a planarized surface; etching a trench (130) on the oxide layer; depositing a barrier layer (135) of tantalum on the oxide layer; depositing a seed layer (140) of gold on the oxide layer; removing the barrier layer of tantalum and seed layer from selected areas (160) of the oxide layer, leaving a seed area (155); and depositing gold on the seed area after removing the barrier layer of tantalum and seed layer from selected areas of the oxide layer; wherein the selected areas are directly on a top surface of the oxide layer. Page 6, line 18 through page 9, line 2, Fig. 1.

Some embodiments include a method of forming a conductor comprising depositing an oxide layer (125) over a planarized surface; etching a trench (130) on the oxide layer; depositing a barrier layer (135) selected from the group consisting of titanium, zirconium, and hafnium on the oxide layer; depositing a seed layer (140) of silver on the oxide layer; removing the barrier layer and seed layer from selected areas (160) of the oxide layer, leaving a seed area (155); and depositing silver on the seed area after removing the barrier layer and seed layer from selected areas of the oxide layer; wherein the selected areas are directly on a top surface of the oxide layer. Page 6, line 18 through page 9, line 2, Fig. 1.

Some embodiments include a method of forming a conductor comprising depositing an oxide layer (125) over a planarized surface; etching a trench (130) on the oxide layer; depositing a barrier layer (135) selected from the group consisting of titanium, zirconium, and hafnium on the oxide layer; depositing a seed layer (140) of copper on the oxide layer; removing the barrier layer and seed layer from selected areas or unused areas (160) of the oxide layer, leaving a seed area (155); and depositing aluminum on the seed area after removing the barrier layer and seed layer from selected areas or unused areas of the oxide layer; wherein the selected areas or the unused areas are directly on a top surface of the oxide layer. Page 6, line 18 through page 9, line 2, Fig. 1.

Some embodiments include a method of forming a conductor comprising depositing a polymer layer (125) over a planarized surface; etching a trench (130) on the polymer layer; depositing a barrier layer (135) selected from the group consisting of titanium, zirconium, and hafnium on the polymer layer; depositing a seed layer (140) selected from the group consisting of gold, silver, and copper on the polymer layer; removing the barrier layer and seed layer from selected areas (160) of the polymer layer, leaving a seed area (155); and depositing a conductor (145) on the seed area after removing the barrier layer and seed layer from selected areas of the polymer layer; wherein the selected areas are directly on a top surface of the polymer layer. Page 6, line 18 through page 9, line 2, Fig. 1.

Some embodiments include a method of forming a conductor comprising depositing a polymer layer (125) over a planarized surface; etching a trench (130) on the polymer layer; depositing a barrier layer (135) selected from the group consisting of titanium, zirconium, and hafnium on the polymer layer; depositing a seed layer (140) of gold on the polymer layer; removing the barrier layer and seed layer from selected areas or unused areas (160) of the polymer layer, leaving a seed area (155); and depositing gold on the seed area after removing the barrier layer and seed layer from selected areas or unused areas of the polymer layer; wherein the selected areas or the unused areas are directly on a top surface of the polymer layer. Page 6, line 18 through page 9, line 2, Fig. 1.

Some embodiments include a method of forming a conductor comprising depositing a polymer layer (125) over a planarized surface; etching a trench (130) on the polymer layer; depositing a barrier layer (135) selected from the group consisting of titanium, zirconium, and hafnium on the polymer layer; depositing a seed layer (140) of silver on the polymer layer; removing the barrier layer and seed layer from selected areas (160) of the polymer layer, leaving a seed area (155); and depositing silver on the seed area after removing the barrier layer and seed layer from selected areas of the polymer layer; wherein the selected areas are directly on a top surface of the polymer layer. Page 6, line 18 through page 9, line 2, Fig. 1.

Some embodiments include a method of forming a conductor comprising depositing a polymer layer (125) over a planarized surface; etching a trench (130) on the polymer layer; depositing a barrier layer (135) selected from the group consisting of titanium, zirconium, and hafnium on the polymer layer; depositing a seed layer (140) of copper on the polymer layer; removing the barrier layer and seed layer from unused areas (160) of the polymer layer, leaving a seed area (155); and depositing copper on the seed area after removing the barrier layer and seed layer from unused areas of the polymer layer; wherein the unused areas are directly on a top surface of the oxide layer. Page 6, line 18 through page 9, line 2, Fig. 1.

Some embodiments include a method of forming a conductor comprising depositing an oxide layer (125) over a planarized surface; etching a trench (130) on the oxide layer; depositing a barrier layer (135) selected from the group consisting of zirconium and titanium on the oxide layer; depositing a seed layer (140) of aluminum-copper on the oxide layer; removing the barrier layer and seed layer from selected areas (160) of the oxide layer, leaving a seed area (155); and depositing a conductor (145) on the seed area after removing the barrier layer and seed layer from selected areas of the oxide layer; wherein the selected areas are directly on a top surface of the oxide layer. Page 6, line 18 through page 9, line 2, Fig. 1.

Some embodiments include a method of forming a conductor comprising depositing an oxide layer (125) over a planarized surface; etching a trench (130) on the oxide layer; depositing a barrier layer (135) of zirconium on the oxide layer; depositing a seed layer (140) of aluminum-copper on the oxide layer; removing the barrier layer and seed layer from selected areas (160) of the oxide layer, leaving a seed area (155); and depositing aluminum on the seed area after removing the barrier layer and seed layer from selected areas of the oxide layer. Page 6, line 18 through page 9, line 2, Fig. 1.

Some embodiments include a method of forming a conductor comprising depositing an oxide layer (125) over a planarized surface; etching a trench (130) on the oxide layer; depositing a barrier layer (135) of titanium on the oxide layer; depositing a seed layer (140) of aluminum-copper on the barrier layer; removing the barrier layer and seed layer from selected areas or unused areas (160) of the oxide layer, leaving a seed

area (155); and depositing aluminum on the seed area after removing the barrier layer and seed layer from selected areas of the oxide layer; wherein the selected areas are directly on a top surface of the oxide layer. Page 6, line 18 through page 9, line 2, Fig. 1.

Some embodiments include a method of forming a conductor comprising depositing an oxide layer (125) over a planarized surface; etching a trench (130) having a top (170) on the oxide layer; depositing a barrier layer (135) of tantalum nitride on the oxide layer; depositing a seed layer (140) of copper directly on the barrier layer of tantalum nitride without a layer between the seed layer of copper and the barrier layer of tantalum nitride; removing the barrier layer and seed layer from selected areas (160) of the oxide layer; depositing a conductor (145) on the seed area leaving a seed area; and depositing a layer (150) of tantalum nitride above the conductor after removing the barrier layer and seed layer from selected areas of the oxide layer; wherein the selected areas are directly on a top surface of the oxide layer. Page 6, line 18 through page 9, line 2, Fig. 1.

Some embodiments include a method of forming a conductor comprising depositing an oxide layer (125) over a planarized surface; etching a trench (130) having a top (170) on the oxide layer; depositing a barrier layer (135) of tantalum nitride on the oxide layer; depositing a seed layer (140) of copper on the barrier layer of tantalum nitride; depositing a seed layer of copper directly on the barrier layer of tantalum nitride without a layer between the seed layer of copper and the barrier layer of tantalum nitride; removing the barrier layer and seed layer from selected areas (160) of the oxide layer, leaving a seed area (155); depositing a layer of copper on the seed area after removing the barrier layer and seed layer from selected areas of the oxide layer; and depositing a layer (150) of tantalum nitride above the layer of copper; wherein the selected areas are directly on a top surface of the oxide layer. Page 6, line 18 through page 9, line 2, Fig. 1.

Some embodiments include a method of forming a conductor comprising depositing an insulator layer (115) over a substrate (105) having at least one device (110); depositing a diffusion barrier layer (120) over the insulator layer; planarizing a surface of the diffusion barrier layer; depositing a different insulator layer (125) over the planarized surface of the diffusion barrier layer; fabricating a connector (165) in the different

insulator layer, wherein fabricating the connector in the different insulator layer includes, etching a trench (130) having a depth on the different insulator layer; depositing a barrier layer (135) on the different insulator layer; depositing a seed layer (140) on the barrier layer; removing the barrier layer and seed layer from selected areas (160) of the different insulator layer, leaving a seed area (155); and depositing a conductor (145) on the seed area of the connector by a selective deposition process after removing the barrier layer and seed layer from selected areas of the different insulator layer; wherein the selected areas are directly on a top surface of the different insulator layer. Page 6, line 18 through page 9, line 10, Fig. 1.

This summary does not provide an exhaustive or exclusive view of the present subject matter, and Appellant refers to the appended claims and its legal equivalents for a complete statement of the invention.

## 6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-7, 12-17, 19-21, 23-25, 27-32, 34-36, 38-41, 56-77, and 186-189 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Havemann et al. (U.S. 6,358,849) in view of Brown et al. (U.S. 6,168,704).

Claims 42-44 and 50-55 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Havemann et al. in view of Brown et al. and Ting et al. (U.S. 5,969,422).

Claims 18, 22, 26, 33, and 37 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Havemann et al. in view of Brown et al. as applied to claims 1-7, 12-17, 19-21, 23-35, 27-32, 34-36, 38-41, 56-77 above, and further in view of Ting et al.

## 7. ARGUMENT

### A) The Applicable Law under 35 U.S.C. §103

The Examiner has the burden under 35 U.S.C. § 103 to establish a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). As part of establishing a *prima facie* case of obviousness, the Examiner must show that some objective teaching in the prior art or some knowledge generally available to one of ordinary skill in the art would lead an individual to combine the relevant teaching of the references. *Id.*

The court in *Fine* stated that:

> Obviousness is tested by "what the combined teaching of the references would have suggested to those of ordinary skill in the art." *In re Keller*, 642 F.2d 413, 425, 208 USPQ 871, 878 (CCPA 1981)). But it "cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination." *ACS Hosp. Sys.*, 732 F.2d at 1577, 221 USPQ at 933. And "teachings of references can be combined *only* if there is some suggestion or incentive to do so."

*Id.* (emphasis in original).

The M.P.E.P. adopts this line of reasoning, stating that

> "To establish a *prima facie* case of obviousness, three base criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Appellant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991))". *M.P.E.P.* § 2142.

The test for obviousness under § 103 must take into consideration the invention as a whole; that is, one must consider the particular problem solved by the combination of elements that define the invention. *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1143, 227 USPQ 543, 551 (Fed. Cir. 1985). The Examiner must, as one of the inquiries

pertinent to any obviousness inquiry under 35 U.S.C. § 103, recognize and consider not only the similarities but also the critical differences between the claimed invention and the prior art. *In re Bond*, 910 F.2d 831, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990), *reh'g denied*, 1990 U.S. App. LEXIS 19971 (Fed. Cir. 1990). Further, the Office Action must provide specific, objective evidence of record for a finding of a suggestion or motivation to combine reference teachings and must explain the reasoning by which the evidence is deemed to support such a finding. *In re Sang Su Lee*, 277 F.3d 1338, 61 USPQ2d 1430 (Fed. Cir. 2002). Further yet, the fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990); MPEP § 2143.01. Finally, the Examiner must avoid hindsight. *In re Bond* at 834.

**B) <u>Discussion of the rejection of the claims under 35 U.S.C. § 103(a) as being obvious over Havemann et al. (U.S. Patent No. 6,358,849) in view of Brown et al. (U.S. Patent No. 6,168,704).</u>**

Claims 1-7, 12-17, 19-21, 23-25, 27-32, 34-36, 38-41, 56-77, and 186-189 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Havemann et al. (U.S. 6,358,849) in view of Brown et al. (U.S. 6,168,704). This rejection is respectfully traversed. Appellant respectfully submits that the Final Office Action has failed to state a *prima facie* case of obviousness with respect to claims 1-7, 12-17, 19-21, 23-25, 27-32, 34-36, 38-41, 56-77, and 186-189 for at least the reasons stated below.

*<u>The proposed combination of Havemann et al. and Brown et al. fails to teach or suggest all of the elements included in each of claims 1-7, 12-17, 19-21, 23-25, 27-32, 34-36, 38-41, 56-77, and 186-189</u>*

Claims 1-7, 12-17, 19-21, 23-25, 27-32, 34-36, 38-41, 56-77, and 186-189 are not obvious in view of the proposed combination of Havemann et al. and Brown et al. because the proposed combination fails to teach or suggest all of the elements included in each of these claims.

For example, claim 1 recites, "wherein the selected areas are directly on a top surface of the insulator," claims 4, 12, and 38 recite, "wherein the unused areas are directly on a top surface of the oxide layer," claims 15, 19, 56, and 67 recite, "wherein the selected areas are directly on a top surface of the oxide layer," claim 23 recites, "wherein the selected areas or the unused areas are directly on a top surface of the oxide layer," claims 27 and 34 recite, "wherein the selected areas are directly on a top surface of the polymer layer," claim 30 recites, "wherein the selected areas or the unused areas are directly on a top surface of the polymer layer," and claim 186 recites, "wherein the selected areas are directly on a top surface of the different insulator layer."

The Final Office Action admits in several places, for example on page 2, that Havemann et al. does not disclose removing the barrier layer and the seed layer from selected areas of the insulation. Appellant agrees. The Final Office Action on page 3 relies in Brown et al. as supplying these elements. However and in contrast, Brown et al., at column 6, lines 14-21, states,

> The barrier metal and copper seed layers 400A and 400B may be blanket-deposited in the opening 405 and <u>on top of a patterned photomask 407</u> (shown in phantom in FIG. 4A) that was used to form the opening 405 in the first place. When the patterned photomask is subsequently removed, the portions of the barrier metal and copper seed layers 400A and 400B <u>overlying the patterned photomask 407</u> are also removed, leaving the barrier metal and copper seed layers 400A and 400B selectively formed only in the opening 405." (emphasis added)

Thus, Brown discloses a barrier metal and copper seed layers on top of a patterned photomask, and when the overlying photomask is removed, portion of the barrier metal and copper seed layers overlaying the photomask are also removed. However, Brown et al. fails to teach or suggest selected areas or unused areas are directly on a top surface of the different layers as quoted in the claims above.

Further, in Brown et al., even after removal of the photomask, the dielectric material 410 is still covered by conductive layer 415, and therefore any areas where the barrier metal layer 400A and the copper seed layer 400B are removed could not be <u>directly</u> on a top surface of the dielectric material 410. Hence, Brown et al. fails to teach

or suggest the elements of claims 1, 4, 12, 15, 19, 23, 27, 30, 34, 38, 56, 67, and 186 as quoted above.

In response to these arguments, the Final Office Action on pages 51-52 states,

> Regarding the applicant's argument that neither Havemann et al. nor Brown et al. discloses removing the barrier and seed layers *from* selected areas of the insulator and that wherein the selected areas are directly on a top surface of the insulator, oxide, or polymer layer, it is noted that the barrier and seed layers are removed from a top surface of the insulator as shown in Figs. 5F-5H, and as disclosed in col. 8, lines 59-67 where the photomask is removed prior to the deposition of the barrier layer and the seed layer, hence the barrier layer and the seed layers are formed directly o the insulating and selected areas are directly on a top surface of the insulator, and since the method of Brown et al. results in removal of the barrier and seed layers from selected areas of the insulator. (Emphasis in original).

Appellant respectfully disagrees. Brown et al. at column 8, line 54 through column 9, line 2 recites,

> As shown in FIG. 5F, the masking layer 515, along with portions of the barrier metal and copper seed layers 525A and 525B overlying the masking layer 515, may be removed. For example, a masking layer 515 formed of photoresist may be removed by being stripped off in a solvent bath. Alternatively, the <u>masking layer 515</u> may be removed before the barrier metal and copper seed layers 525A and 525B are formed (for example, by being deposited) <u>to make a conductive path through the barrier metal and copper seed layers 525A and 525B in the opening 520 and through the conductive layer 500</u>. <u>The barrier metal and copper seed layers 525A and 525B shown in FIG. 5D would then be deposited directly on the conductive layer 500</u>, since the masking layer 515 would have been removed before the barrier metal and copper seed layers 525A and 525B were deposited. (Emphasis added).

As underlined above, Brown et al. clearly discloses barrier and seed layers shown in Fig. 5F are deposited directly on a **conductive layer 500**, which separates the dielectric layer 505 from the barrier and seed layer. Brown et al. goes on to describe that

this particular arrangement is used to "make a conductive path through the barrier metal and copper seed layers 525A and 525B in the opening 520 and through the conductive layer 500." Thus, Brown et al. clearly fails to disclose for example, "wherein the selected areas are <u>directly on a top surface of the insulator</u>," as recited in claim 1. (Emphasis added). Therefore, Fig. 5 and the disclosure in Brown et al. contradict the arguments presented in Final Office Action.

In a further response to Appellant's statement above that "In Brown et al., even after removal of the photomask, the dielectric material 410 is still covered by conductive layer 415, and therefore any areas where the barrier metal layer 400A and the copper seed layer 400B are removed could not be <u>directly</u> on a top surface of the dielectric material 410," the Advisory Action[1] on page 2 states,

> Applicant's argument that Brown et al. disclose that the selected areas that are removed could not be directly on a top surface of the dielectric material 410, it is noted that the examiner did not identify 410 as the dielectric material. but rather the claims language requires "an insulator over a planarized surface" and with regards to the series of figures 4, the insulator is dielectric material 420, and the selected areas that are removed are directly on a top surface of the dielectric mater, hence the limitation is taught and suggested by Brown et al.

Appellant disagrees. The Final Office Action on page 3 states, "Brown et al. discloses a method of forming a conductor that comprises etching a trench 405 having a depth <u>on an insulator (col. 6, lines 3-6)</u>." (Emphasis added). Brown et al. at column 6, lines 3-6 states,

> As shown in FIG. 4A, a barrier metal layer 400A and a copper seed layer 400B may be selectively formed only in an opening (such as a trench) 405 that is formed in <u>a layer of dielectric material 410</u> disposed on a structure layer 412. (Emphasis added).

1 *See* the "Advisory Action Before the Filing of an Appeal Brief" mailed December 27,2005 in the 09/259,849 application.

Thus, the Final Office Action clearly refers to layer 410 of Brown et al. in an attempt to supply an insulator as recited in the claims. Further, with respect to layer 420, Brown et al. at column 6, lines 34-41 states,

> Again, the portions of the barrier metal and copper seed layers 400A and 400B <u>overlying the conductive layer 415</u> would effectively be removed, by being converted into a silicide <u>that is later selectively covered by an insulating layer 420</u> (shown in phantom in FIG. 4A), leaving the unconverted and uncovered barrier metal and copper seed layers 400A and 400B selectively formed only in the opening 405. (underlining added)

Therefore, layer 420 in Brown et al. <u>covers</u> the silicide. This clearly fails to teach the elements included in, for example, claim 1 of:

> <u>depositing a barrier layer on the insulator;</u>
> <u>depositing a seed layer directly on the barrier layer;</u>
> removing the barrier layer and seed layer <u>from selected areas of the insulator</u>, leaving a seed area; and
> depositing a conductor on the seed area by a selective deposition process after removing the barrier layer and seed layer from selected areas of the insulator;
> <u>wherein the selected areas are directly on a top surface of the insulator.</u>

Thus, neither Havemann et al. nor Brown et al., either alone or in combination, teach or suggest each of the elements of claims 1, 4, 12, 15, 19, 23, 27, 30, 34, 38, 56, 67, and 186. Because the Final Office Action relies on the proposed combination of Havemann et al. and Brown et al. in forming the 35 U.S.C. 130(a) rejection of these claims, and since the proposed combination of Havemann et al. and Brown et al. fails to teach or suggest all of the elements included in these claims, the Final Office Action fails to state a *prima facie* case of obviousness with respect to these claims, and so the Appellant respectfully requests withdrawal of the rejection and reconsideration and allowance of claims 1, 4, 12, 15, 19, 23, 27, 30, 34, 38, 56, 67, and 186.

Claims 2-3, 5-7, 13-14, 16-17, 20-21, 24-25, 28-29, 31-32, 35-36, 39-41, 57-66, 68-77, and 187-189 are dependent on one of claims 1, 4, 12, 15, 19, 23, 27, 30, 34, 38, 56, 67, and 186 respectively. For reasons analogous to those stated above and elements in the claims, Appellant submits that the Final Office Action fails to state a *prima facie* case of obviousness with respect to these claims, and therefore respectfully requests

withdrawal of the rejections and reconsideration and allowance of claims 1-7, 12-17, 19-21, 23-25, 27-32, 34-36, 38-41, 56-77, and 186-189.

In addition, the Final Office Action repeatedly, for example on pages 7-8 with regards to claim 13, states or makes statement to the effect that,

> Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to vary the depth of the trench, thus varying the depth to which the barrier layer is deposited as there is no statement denoting the critically of the depth to which the barrier layer is deposited.

Further the Final Office Action repeatedly, for example on page 10 with respect to claim 15, states or makes statements to the effect that,

> Furthermore, it would have been within the scope of one of ordinary skill in the art at the time the invention was made that gold may be used as an alternative to copper or aluminum although copper is preferred over gold, and as Brown et al. discloses that the use of gold has been considered in semiconductor interconnections and disclosed examples and preferred embodiments do not constitute a teaching away from a broader disclosure or nonpreferred embodiments.

Further, for example on page 13 with respect to claim 19, the Final Office Action recites,

> Furthermore, it would have been within the scope of one of ordinary skill in the art at the time the invention was made that silver may be used as an alternative to copper or aluminum although copper is preferred over silver, and as Brown et al. discloses that the use of gold has been considered in semiconductor interconnections and disclosed examples and preferred embodiments do not constitute a teaching away from a broader disclosure or nonpreferred embodiments.

Appellant disagrees with each of the above or similar statements made throughout the Final Office Action, and Appellant further submits that these statements are unsupported by the references and therefore are within the personal knowledge of the Examiner. Further, no affidavits as required by MPEP § 2144.03 have been provided in support of these statements made in the Final Office Action. Thus, these statements as referred to above represent statements unsupported by a cited reference or an affidavit, and thus, Appellant submits that the claims to which these statements are directed are

therefore not obvious, and thus patentable, over the 35 U.S.C. § 103(a) rejection against these claims.

*The Final Office Action fails to state a proper basis for forming the proposed combination of Havemann et al. with Brown et al.*

Appellant respectfully submits that the Final Office Action fails to meet the requirements as noted above for forming the proposed combination of Havemann et al. with Brown et al. and so fails to state a *prima facie* case of obviousness with respect to the 35 U.S.C. § 103(a) rejection of claims 1-7, 12-17, 19-21, 23-25, 27-32, 34-36, 38-41, 56-77, and 186-189.

For example, the Final Office Action on pages 3-4 states,

> Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to remove the barrier layer and the seed layer from selected areas and to deposit the conductor by a selective deposition process only in those areas left after the removal of the barrier layer and the seed layer in the invention of Havemann et al. for the disclosed intended purpose of Brown et al. of reducing the manufacturing cost, reducing consumption of electroplating solution and CMP consumables, reducing the amount of post-metallization deposition CMP needed and reducing the amount of hazardous effluents as disclosed by Brown et al. in col. 16, lines 42-67 and col. 17, lines 1-24. (emphasis added)

However, Appellant submits that these statements are not supported by the record. For example, Brown et al. in the portions relied on by the Final Office Action describe "selectively electrochemically depositing copper," wherein Brown et al. at column 16, lines 42-50 states,

> Any of the above-disclosed embodiments of a method for selectively electrochemically depositing copper according to the present invention enables a copper layer to be selectively deposited only to desired areas. This decreases the cost of the raw materials and the amount of processing needed to remove the copper from undesired areas when compared to conventional dual-damascene copper process flows, as shown in FIGS. 2A-2E, and conventional single-

> damascene copper process flows, as shown in FIGS. 1A-1E.

Thus, any saving that might be taught or suggested to by Brown et al. (while Appellant does not admit it to be so) relate to the selective deposition of the copper layer, and are not related "to remove the barrier layer and the seed layer form [sic] selected areas" as recited in the Final Office Action. Further, the cited portion of Brown et al. in part states at column 17, lines 17-22 that, "Finally, in any of the above-disclosed embodiments of a method for selectively electrochemically depositing copper according to the present invention, it <u>is not necessary to etch the barrier or seed layers</u>, which can be extremely difficult and time consuming." (Emphasis added). Thus, the statement on page 3 of the Final Office Action, "to remove the barrier and seed layer form [sic] selected areas and to deposit the conductor . . . " in support of the combination of Havemann et al. and Brown et al. is directly contradicted by the disclosure in Brown et al.

Further, Brown et al. at column 6, lines 33-37, states, "portions of the barrier metal and copper seed layers 400A and 400B overlying the conductive layer 415 would <u>effectively be removed, by being converted into a silicide</u> that is later selectively covered by an insulating layer 420." (Emphasis added). Appellant respectfully submits that Brown et al. fails to describe how any of *these* processes relate to "reducing the manufacturing cost, reducing consumption of electroplating solution and CMP consumables, reducing the amount of post-metallization deposition CMP needed and reducing the amount of hazardous effluents." as recited in the Final Office Action. Appellant respectfully submits that the reasoning of the Final Office Action is defective, so the evidence does not support the finding. Thus, by failing to meet the standard of *In re* Sang Su Lee, the Final Office Action fails to state a *prima facie* case of obviousness with respect to claims 1-7, 12-17, 19-25, 27-32, 34-36, 38-44, 50-77, and 186-189.

Still further, Havemann et al. is concerned with CMP processing having manufacturability problems (see column 1, lines 50-51) and at column 3, lines 42-49 states,

> (10) Remove the portion of copper and TiN barrier outside of the interconnect trenches by CMP; the CMP also planarizes any bumpiness in

> the plated copper. Initially use a hard pad to planarize, and then follow with a soft pad. ARC 126 acts as a CMP polish stop; copper polishes faster than the silicon oxynitride. The remaining copper forms interconnects 160; see FIG. 1g.

Thus, Havemann et al. removes the copper and TiN outside of the interconnect trenches by CMP as a way of planarizing any bumpiness in the plated copper, and therefore the method of Brown et al. of selective deposition of the copper destroys the stated purpose of Havemann et al., that being elimination of manufacturability problems by the use of CMP on copper outside the interconnect trenches. Because the statements in the Final Office Action in support of the combination of Havemann et al. and Brown et al. are not supported by the documents themselves, the Final Office Action fails to state a *prima facie* case of obviousness with respect to claims 1-7, 12-17, 19-21, 23-25, 27-32, 34-36, 38-41, 56-77, and 186-189.

Another argument made in Final Office Action and again in the Advisory Action, in an attempt to justify the proposed combination of Havemann et al. and Brown et al., states that Brown et al. in column 1, lines 20-46 discussed the use of different materials such as gold and silver as "alternatives" to copper. Applicant respectfully disagrees. A careful review of the cited portion of Brown et al. reveals that these metals present various problems (such as corrosion in silver) and constraints (such as cost) when being used in the formation of semiconductor devices, and therefore present various tradeoffs with respect to conductivity, cost, and difficulty in manufacturability. Thus, Brown et al. fails to disclose that these metals are alternatives to one another as suggested in the Final Office Action. In fact, Brown et al. teaches away from these materials as alternatives to one another in particular applications based on one or more of the characteristics discussed in the cited portion of the specification of Brown et al.

Thus, Brown et al. discuss various <u>problems and constraints</u> when using alternative material in the formation of semiconductor devices, and so Brown et al. teaches away from the use of one or more of these materials as alternatives in particular applications based on these characteristics. The proposition that these material are "alternatives" is not supported by, and is contrary to, the disclosure of the cited

references. Brown et al. actually discourages certain applications of these materials based on the particular application, and therefore the disclosure in Brown et al. does not support forming the proposed combination of Havemann et al. with Brown et al. as suggested by the Final Office Action.

Because the basis for forming the proposed combination of Havemann et al. and Brown et al. as stated in the Final Office Action is not supported by the disclosure in the references themselves, the Final Office Action fails to state a *prima facie* case of obviousness in rejecting claims 1-7, 12-17, 19-21, 23-25, 27-32, 34-36, 38-41, 56-77, and 186-189, because the Final Office Action fails to show the desirability[2] of forming the combination of Havemann et al. and Brown et al.

For at least the reasons stated above, Appellant respectfully requests withdrawal of the rejection and reconsideration and allowance of claims 1-7, 12-17, 19-21, 23-25, 27-32, 34-36, 38-41, 56-77, and 186-189.

**C) <u>Discussion of the rejection of the claims under 35 U.S.C. § 103(a) as being obvious over Havemann et al. (U.S. Patent No. 6,358,849) in view of Brown et al. (U.S. Patent No. 6,168,704) and Ting et al. (U.S. Patent No. 5,969,422).</u>**

Claims 42-44 and 50-55 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Havemann et al. in view of Brown et al. and Ting et al. (U.S. 5,969,422). Further, claims 18, 22, 26, 33, and 37 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Havemann et al. in view of Brown et al. as applied to claims 1-7, 12-17, 19-21, 23-35, 27-32, 34-36, 38-41, 56-77 above, and further in view of Ting et al. Each of these rejections is respectfully traversed. Appellant respectfully submits that the Final Office Action has failed to state a *prima facie* case of obviousness with respect to claims 42-44 and 50-55 and claims 18, 22, 26, 33, and 37 for at least the reasons stated below.

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2 The fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests <u>the desirability</u> of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990); MPEP § 2143.01. (emphasis added).

*The proposed combination of Havemann et al., Brown et al., and Ting et al. fails to teach or suggest all of the elements included in each of claims 42-44 and 50-55 and claims 18, 22, 26, 33, and 37.*

Claims 42-44 and 50-55 and claims 18, 22, 26, 33, and 37 are not obvious in view of the proposed combination of Havemann et al., Brown et al., and Ting et al. because the proposed combination fails to teach or suggest all of the elements included in each of these claims.

For example, claims 42 and 50 recite, "wherein the selected areas are directly on a top surface of the oxide layer." Claims 43-44 and 51-55 depend from claims 42 and 50 respectively, and therefore include all the elements recited in the claim from which they depend. For reasons analogous to those argued above with regards to claims 1-7, 12-17, 19-21, 23-25, 27-32, 34-36, 38-41, 56-77, and 186-189, neither Havemann et al. nor Brown et al. teach or suggest these elements of claims 42 and 50 as quoted above. The Final Office Action does not rely on, and fails to point out in Ting et al., any teaching or suggestion of these elements missing in Havemann et al. and Brown et al. as recited in claims 42 and 50. Thus, neither Havemann et al., nor Brown et al., nor Ting et al., either alone or in combination, teach or suggest all of the elements in claims 42-44 and 50-55.

Further, claims 18, 22, 26, 33, and 37 depend from claims 15, 19, 23, 30, and 34 respectively and therefore include all the elements recited in the claim from which they depend. As argued above with regards to claims 15, 19, 23, 30, and 34, neither Havemann et al. nor Brown et al. teach or suggest all of the elements as recited in claims 15, 19, 23, 30, and 34, and so fail to teach or suggest all of the elements in claims 18, 22, 26, 33, and 37. The Final Office Action does not rely on, and fails to point out in Ting et al., any teaching or suggestion of these elements missing in Havemann et al. and Brown et al. as recite in claims 15, 19, 23, 30, and 34. Thus, neither Havemann et al., nor Brown et al., nor Ting et al., either alone or in combination, teach or suggest all of the elements in claims 18, 22, 26, 33, and 37.

*The Final Office Action fails to state a proper basis for forming the proposed combination of Havemann et al., Brown et al., and Ting et al.*

In addition, the Final Office Action does not provide any additional motive for combining Havemann et al. with Brown et al. with regards to claims 18, 22, 26, 33, 37, 42-44, and 50-55.

Thus, for the reasons argued above, the Final Office Action has fails to state a *prima facie* case of obviousness with respect to claims 18, 22, 26, 33, 37, 42-44, and 50-55 because the Final Office Action fails to show a suggestion for the desirability to combine the referenced of Havemann et al., Brown et al., and Ting et al.

For at least the reasons stated above, Appellant respectfully requests withdrawal of the rejections and reconsideration and allowance of claims 18, 22, 26 33, 37, 42-44, and 50-55.

## 8. SUMMARY

For at least the reasons argued above, claims 1-7, 12-17, 19-21, 23-25, 27-32, 34-36, 38-41, 56-77, and 186-189 were not properly rejected under 35 U.S.C. § 103(a) as being unpatentable over Havemann et al. (U.S. 6,358,849) in view of Brown et al. (U.S. 6,168,704). Further, claims 42-44 and 50-55 were not properly rejected under 35 U.S.C. § 103(a) as being unpatentable over Havemann et al. in view of Brown et al. and Ting et al. (U.S. 5,969,422). And further, claims 18, 22, 26, 33, and 37 were not properly rejected under 35 U.S.C. § 103(a) as being unpatentable over Havemann et al. in view of Brown et al. as applied to claims 1-7, 12-17, 19-21, 23-35, 27-32, 34-36, 38-41, 56-77 above, and further in view of Ting et al.

It is further respectfully submitted that the cited documents do not render the claims obvious, and that the claims are patentable over the cited documents. Reversal of the rejections and allowance of all pending claims is respectfully requested.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 13 day of April, 2006.

KATE GANNON [signature]
Name Signature

## CLAIMS APPENDIX

The Claims on Appeal

1. A method of forming a conductor comprising:

depositing an insulator over a planarized surface;

etching a trench having a depth on the insulator;

depositing a barrier layer on the insulator;

depositing a seed layer directly on the barrier layer;

removing the barrier layer and seed layer from selected areas of the insulator, leaving a seed area; and

depositing a conductor on the seed area by a selective deposition process after removing the barrier layer and seed layer from selected areas of the insulator,

wherein the selected areas are directly on a top surface of the insulator.

2. The method of claim 1, wherein depositing the barrier layer on the insulator comprises:

depositing the barrier layer on the insulator by physical vapor-deposition.

3. The method of claim 1, wherein etching a trench on the insulator comprises:

etching the trench to a depth of about equal to the depth of the insulator.

4. A method of forming a conductor comprising:

depositing an oxide layer over a planarized surface;

etching a trench on the oxide layer;

depositing a barrier layer on the oxide layer;

depositing a seed layer on the barrier layer without a layer between the seed layer and the barrier layer;

removing the barrier layer and seed layer from unused areas of the oxide layer, leaving a seed area; and

depositing a conductor on the seed area after removing the barrier layer and seed layer from unused areas of the oxide layer;

wherein the unused areas are directly on a top surface of the oxide layer.

5. The method of claim 4, wherein depositing an oxide layer over a planarized surface comprises:

depositing a silicon dioxide layer over the planarized surface.

6. The method of claim 4, wherein depositing an oxide layer over a planarized surface comprises:

depositing a fluorinated silicon oxide layer over the planarized surface.

7. The method of claim 4, wherein depositing a seed layer on the barrier layer comprises:

depositing the seed layer on the barrier layer by physical vapor-deposition.

12. A method of forming a conductor comprising:

depositing an oxide layer over a planarized surface;

etching a trench on the oxide layer;

depositing a barrier layer of tantalum on the oxide layer;

depositing a seed layer selected from the group consisting of gold, silver, and copper on the oxide layer;

removing the barrier layer of tantalum and seed layer from unused areas of the oxide layer, leaving a seed area; and

depositing a conductor on the seed area after removing the barrier layer of tantalum and seed layer from unused areas of the oxide layer;

wherein the unused areas are directly on a top surface of the oxide layer.

13. The method of claim 12, wherein depositing a barrier layer of tantalum on the oxide layer comprises:

depositing the barrier layer of tantalum to a depth of between fifty angstroms and one-thousand angstroms.

14. The method of claim 12, wherein depositing the barrier layer of tantalum and gold on the oxide layer comprises:

depositing the barrier layer by physical vapor-deposition.

15. A method of forming a conductor comprising:

depositing an oxide layer over a planarized surface;

etching a trench on the oxide layer;

depositing a barrier layer of tantalum on the oxide layer;

depositing a seed layer of gold on the oxide layer;

removing the barrier layer of tantalum and seed layer from selected areas of the oxide layer, leaving a seed area; and

depositing gold on the seed area after removing the barrier layer of tantalum and seed layer from selected areas of the oxide layer;

wherein the selected areas are directly on a top surface of the oxide layer.

16. The method of claim 15, wherein depositing a barrier layer of tantalum on the oxide layer comprises:

depositing the barrier layer of tantalum to a depth of between fifty angstroms and one-thousand angstroms.

17. The method of claim 15, wherein depositing the barrier layer of tantalum and gold on the oxide layer comprises:

depositing the barrier layer of tantalum by physical vapor-deposition.

18. The method of claim 15, wherein depositing gold on the seed area comprises:

depositing gold on the seed area by electroless plating.

19. A method of forming a conductor comprising:

depositing an oxide layer over a planarized surface;

etching a trench on the oxide layer;

depositing a barrier layer selected from the group consisting of titanium, zirconium, and hafnium on the oxide layer;

depositing a seed layer of silver on the oxide layer;

removing the barrier layer and seed layer from selected areas of the oxide layer, leaving a seed area; and

depositing silver on the seed area after removing the barrier layer and seed layer from selected areas of the oxide layer;

wherein the selected areas are directly on a top surface of the oxide layer.

20. The method of claim 19, wherein depositing the barrier layer of titanium and silver on the oxide layer comprises:

depositing the barrier layer by physical vapor-deposition.

21. The method of claim 19, wherein depositing a seed layer of titanium and silver on the oxide layer comprises:

depositing the seed layer of titanium and silver to a depth of between fifty angstroms and two-thousand angstroms.

22. The method of claim 19, wherein depositing silver on the seed area comprises:

depositing silver on the seed area by electroless plating.

23. A method of forming a conductor comprising:

depositing an oxide layer over a planarized surface;

etching a trench on the oxide layer;

depositing a barrier layer selected from the group consisting of titanium, zirconium, and hafnium on the oxide layer;

depositing a seed layer of copper on the oxide layer;

removing the barrier layer and seed layer from selected areas or unused areas of the oxide layer, leaving a seed area; and

depositing aluminum on the seed area after removing the barrier layer and seed layer from selected areas or unused areas of the oxide layer;

wherein the selected areas or the unused areas are directly on a top surface of the oxide layer.

24. The method of claim 23, wherein depositing a barrier layer selected from the group consisting of titanium, zirconium, and hafnium on the oxide layer comprises:

depositing the barrier layer to a depth of between fifty angstroms and one-thousand angstroms.

25. The method of claim 23, wherein depositing the barrier layer of titanium and aluminum on the oxide layer comprises:

depositing the barrier layer by physical vapor-deposition.

26. The method of claim 23, wherein depositing copper on the seed area comprises:

depositing aluminum on the seed area by selective chemical vapor-deposition (CVD).

27. A method of forming a conductor comprising:

depositing a polymer layer over a planarized surface;

etching a trench on the polymer layer;

depositing a barrier layer selected from the group consisting of titanium, zirconium, and hafnium on the polymer layer;

depositing a seed layer selected from the group consisting of gold, silver, and copper on the polymer layer;

removing the barrier layer and seed layer from selected areas of the polymer layer, leaving a seed area; and

depositing a conductor on the seed area after removing the barrier layer and seed layer from selected areas of the polymer layer;

wherein the selected areas are directly on a top surface of the polymer layer.

28. The method of claim 27, wherein depositing a barrier layer selected from the group consisting of titanium, zirconium, and hafnium on the oxide layer comprises:

depositing the barrier layer to a depth of between fifty angstroms and one-thousand angstroms.

29. The method of claim 27, wherein depositing a barrier layer selected from the group consisting of titanium, zirconium, and hafnium on the polymer layer comprises:

depositing the barrier layer by physical vapor-deposition.

30. A method of forming a conductor comprising:

depositing a polymer layer over a planarized surface;

etching a trench on the polymer layer;

depositing a barrier layer selected from the group consisting of titanium, zirconium, and hafnium on the polymer layer;

depositing a seed layer of gold on the polymer layer;

removing the barrier layer and seed layer from selected areas or unused areas of the polymer layer, leaving a seed area; and

depositing gold on the seed area after removing the barrier layer and seed layer from selected areas or unused areas of the polymer layer;

wherein the selected areas or the unused areas are directly on a top surface of the polymer layer.

31. The method of claim 30, wherein depositing a barrier layer selected from the group consisting of titanium, zirconium, and hafnium on the oxide layer comprises:

depositing the barrier layer to a depth of between fifty angstroms and one-thousand angstroms.

32. The method of claim 30, wherein depositing a barrier layer selected form the group consisting of titanium, zirconium, and hafnium on the oxide layer comprises:

depositing the barrier layer by physical vapor-deposition.

33. The method of claim 30, wherein depositing gold on the seed area comprises:

depositing gold on the seed area by electroless plating.

34. A method of forming a conductor comprising:

depositing a polymer layer over a planarized surface;

etching a trench on the polymer layer;

depositing a barrier layer selected from the group consisting of titanium, zirconium, and hafnium on the polymer layer;

depositing a seed layer of silver on the polymer layer;

removing the barrier layer and seed layer from selected areas of the polymer layer, leaving a seed area; and

depositing silver on the seed area after removing the barrier layer and seed layer from selected areas of the polymer layer;

wherein the selected areas are directly on a top surface of the polymer layer.

35. The method of claim 34, wherein depositing a barrier layer selected from the group consisting of titanium, zirconium, and hafnium on the oxide layer comprises:

depositing the barrier layer to a depth of between fifty angstroms and one-thousand angstroms.

36. The method of claim 34, wherein depositing a barrier layer selected from the group consisting of titanium, zirconium, and hafnium on the polymer layer comprises:

depositing the barrier layer by physical vapor-deposition.

37. The method of claim 34, wherein depositing silver on the seed area comprises:
depositing silver on the seed area by electroless plating.

38. A method of forming a conductor comprising:
depositing a polymer layer over a planarized surface;
etching a trench on the polymer layer;
depositing a barrier layer selected from the group consisting of titanium, zirconium, and hafnium on the polymer layer;
depositing a seed layer of copper on the polymer layer;
removing the barrier layer and seed layer from unused areas of the polymer layer, leaving a seed area; and
depositing copper on the seed area after removing the barrier layer and seed layer from unused areas of the polymer layer;
wherein the unused areas are directly on a top surface of the oxide layer.

39. The method of claim 38, wherein depositing a barrier layer selected from the group consisting of titanium, zirconium, and hafnium on the polymer layer comprises:
depositing the barrier layer to a depth of between fifty angstroms and one-thousand angstroms.

40. The method of claim 38, wherein depositing a barrier layer selected from the group consisting of titanium, zirconium, and hafnium on the polymer layer comprises:
depositing the barrier layer by physical vapor-deposition.

41. The method of claim 38, wherein depositing copper on the seed area comprises:
depositing copper on the seed area by electroless plating.

42. A method of forming a conductor comprising:
depositing an oxide layer over a planarized surface;
etching a trench on the oxide layer;

depositing a barrier layer selected from the group consisting of zirconium and titanium on the oxide layer;

depositing a seed layer of aluminum-copper on the oxide layer;

removing the barrier layer and seed layer from selected areas of the oxide layer, leaving a seed area; and

depositing a conductor on the seed area after removing the barrier layer and seed layer from selected areas of the oxide layer;

wherein the selected areas are directly on a top surface of the oxide layer.

43. The method of claim 42, wherein depositing a barrier layer selected from the group consisting of zirconium and titanium on the oxide layer comprises:

depositing the barrier layer to a depth of between fifty angstroms and one-thousand angstroms.

44. The method of claim 42, wherein depositing the barrier layer selected from the group consisting of zirconium and titanium on the oxide layer comprises:

depositing the barrier layer by physical vapor-deposition.

50. A method of forming a conductor comprising:

depositing an oxide layer over a planarized surface;

etching a trench on the oxide layer;

depositing a barrier layer of titanium on the oxide layer;

depositing a seed layer of aluminum-copper on the barrier layer;

removing the barrier layer and seed layer from selected areas or unused areas of the oxide layer, leaving a seed area; and

depositing aluminum on the seed area after removing the barrier layer and seed layer from selected areas of the oxide layer;

wherein the selected areas are directly on a top surface of the oxide layer.

51. The method of claim 50, wherein depositing a barrier layer of titanium on the oxide layer comprises:

depositing the barrier layer to a depth of between fifty angstroms and one-thousand angstroms.

52. The method of claim 50, wherein depositing a barrier layer of titanium on the oxide layer comprises:

depositing the barrier layer by physical vapor-deposition.

53. The method of claim 50, wherein depositing aluminum on the seed area comprises:

depositing aluminum on the seed area by chemical vapor-deposition.

54. The method of claim 50, wherein depositing a seed layer of aluminum-copper on the barrier layer comprises:

depositing the seed layer of aluminum-copper on the barrier layer by chemical vapor-deposition.

55. The method of claim 50, wherein depositing aluminum on the seed area comprises:

depositing an amount of aluminum sufficient to fill the trench.

56. A method of forming a conductor comprising:

depositing an oxide layer over a planarized surface;

etching a trench having a top on the oxide layer;

depositing a barrier layer of tantalum nitride on the oxide layer;

depositing a seed layer of copper directly on the barrier layer of tantalum nitride without a layer between the seed layer of copper and the barrier layer of tantalum nitride;

removing the barrier layer and seed layer from selected areas of the oxide layer;

depositing a conductor on the seed area leaving a seed area; and

depositing a layer of tantalum nitride above the conductor after removing the barrier layer and seed layer from selected areas of the oxide layer;

wherein the selected areas are directly on a top surface of the oxide layer.

57. The method of claim 56, wherein depositing a barrier layer of tantalum nitride on the oxide layer comprises:

depositing approximately one-hundred angstroms of tantalum nitride.

58. The method of claim 56, wherein depositing a seed layer of copper on the tantalum nitride layer comprises:

depositing approximately five-hundred angstroms of copper on the tantalum nitride layer.

59. The method of claim 56, wherein depositing a barrier layer of tantalum nitride on the oxide layer comprises:

depositing the barrier layer of tantalum nitride by a non-anisotropic deposition technique.

60. The method of claim 56, wherein depositing a seed layer of copper on the barrier layer of tantalum nitride comprises:

depositing the seed layer of copper on the tantalum nitride layer by a non-anisotropic deposition technique.

61. The method of claim 56, wherein depositing a barrier layer of tantalum nitride on the oxide layer comprises:

depositing the barrier layer of tantalum nitride to a depth of between fifty angstroms and one-thousand angstroms.

62. The method of claim 56, wherein depositing a barrier layer of tantalum nitride on the oxide layer comprises:

depositing the barrier layer of tantalum nitride on the oxide layer by chemical vapor-deposition.

63. The method of claim 56, wherein depositing a seed layer of copper on the layer of tantalum nitride comprises:

depositing the seed layer copper on the barrier layer to a depth of approximately five-hundred angstroms below the top of the trench.

64. The method of claim 56, wherein depositing a barrier layer of tantalum nitride above the conductor comprises:

depositing the barrier layer of tantalum nitride above the conductor to a depth of approximate five-hundred angstroms.

65. The method of claim 56, wherein depositing an oxide layer over a planarized surface comprises:

depositing a silicon dioxide layer over the planarized surface.

66. The method of claim 56, wherein depositing an oxide layer over a planarized surface comprises:

depositing a fluorinated silicon oxide layer over the planarized surface.

67. A method of forming a conductor comprising:

depositing an oxide layer over a planarized surface;

etching a trench having a top on the oxide layer;

depositing a barrier layer of tantalum nitride on the oxide layer;

depositing a seed layer of copper on the barrier layer of tantalum nitride;

depositing a seed layer of copper directly on the barrier layer of tantalum nitride without a layer between the seed layer of copper and the barrier layer of tantalum nitride;

removing the barrier layer and seed layer from selected areas of the oxide layer, leaving a seed area;

depositing a layer of copper on the seed area after removing the barrier layer and seed layer from selected areas of the oxide layer; and

depositing a layer of tantalum nitride above the layer of copper;

wherein the selected areas are directly on a top surface of the oxide layer.

68. The method of claim 67, wherein depositing a barrier layer of tantalum nitride on the oxide layer comprises:

depositing approximately one-hundred angstroms of tantalum nitride.

69. The method of claim 67, wherein depositing a seed layer of copper on the oxide layer comprises:

depositing approximately five-hundred angstroms of copper on the oxide layer.

70. The method of claim 67, wherein depositing a barrier layer of tantalum nitride on the oxide layer comprises:

depositing the barrier layer of tantalum nitride by a non-anisotropic deposition technique.

71. The method of claim 67, wherein depositing a barrier layer of tantalum nitride on the oxide layer comprises:

depositing the barrier layer of tantalum nitride to a depth of between fifty angstroms and one-thousand angstroms.

72. The method of claim 67, wherein depositing a barrier layer of tantalum nitride on the oxide layer comprises:

depositing the barrier layer of tantalum nitride on the oxide layer by chemical vapor-deposition.

73. The method of claim 67, wherein depositing a layer of copper on the seed area comprises:

depositing the layer of copper on the seed area by chemical vapor-deposition.

74. The method of claim 67, wherein depositing a layer of copper on the seed area comprises:

depositing the layer of copper on the seed area to a depth of approximately five-hundred angstroms below the top of the trench.

75. The method of claim 67, wherein depositing a layer of tantalum nitride above the copper comprises:

depositing the layer of tantalum nitride above the copper to a depth of approximate five-hundred angstroms.

76. The method of claim 67, wherein depositing an oxide layer over a planarized surface comprises:

depositing a silicon dioxide layer over the planarized surface.

77. The method of claim 67, wherein depositing an oxide layer over a planarized surface comprises:

depositing a fluorinated silicon oxide layer over the planarized surface.

186. A method comprising:

depositing an insulator layer over a substrate having at least one device;

depositing a diffusion barrier layer over the insulator layer;

planarizing a surface of the diffusion barrier layer;

depositing a different insulator layer over the planarized surface of the diffusion barrier layer;

fabricating a connector in the different insulator layer, wherein fabricating the connector in the different insulator layer includes,

etching a trench having a depth on the different insulator layer;

depositing a barrier layer on the different insulator layer;

depositing a seed layer on the barrier layer;

removing the barrier layer and seed layer from selected areas of the different insulator layer, leaving a seed area; and

depositing a conductor on the seed area of the connector by a selective deposition process after removing the barrier layer and seed layer from selected areas of the different insulator layer;

wherein the selected areas are directly on a top surface of the different insulator layer.

187. The method of claim 186 wherein depositing the seed layer on the barrier layer includes depositing the seed layer selected from the group consisting of gold, silver, and copper on the barrier layer.

188. The method of claim 186, wherein depositing the barrier layer on the different insulator layer includes depositing the barrier layer on the different insulator layer by physical vapor-deposition.

189. The method of claim 186, wherein depositing the different insulator layer over the planarized surface of the diffusion barrier layer includes depositing an oxide layer over the planarized surface of the diffusion barrier layer.

# EVIDENCE APPENDIX

None.

# RELATED PROCEEDINGS APPENDIX

None.